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/Scott W. Brim/ August 12, 2009
Signature Date

Our Case No. 10519/804

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Chang, et al.	
Serial No.:	10/679,000	Examiner: Shen-Jen Tsai
Filing Date:	Oct. 2, 2003	Group Art Unit No.: 2186
For:	Method and Apparatus for Managing the Integrity of Data in Non-Volatile Memory System	Confirmation No.: 8920

RESPONSE TO NOTICE OF NON-COMPLIANT BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandra, VA 22313-1450

Dear Sir:

In response to the Notice of Non-Compliant Brief dated July 14, 2009, Applicants submit the following replacement Summary of the Claim Subject Matter and Claims Appendix sections.

Summary of the Claimed Subject Matter

Independent claim 1 is directed to a method of storing error-correction encoded data stored in a non-volatile memory system (100), such as a flash memory system. (See Figs. 3a-3c and Page 8, line 19-Page 13, line 26). According to the claimed method, a page (400) of data to be written into non-volatile memory (124) is divided into two or more segments of data (406, 408; 426a, 426b, 426c; 446a, 446b, 444). (See Figs. 4a-4c and Page 13, line 27-Page 16, line 18). The page corresponds to the smallest unit of programming in the non-volatile flash memory. (See Page 12, lines 4-16). One of the segments (406; 426a; 446a) within the page is encoded according to a first error-correction code (ECC) algorithm, and another segment (408; 426b; 446b) within the page is separately encoded according to a second ECC algorithm. (See Page 20, line 29-Page 21, line 3). The page is then programmed with the encoded data of these two segments. (See Page 12, lines 4-16 and Page 31, lines 21-26).

Independent claim 11 is directed to a memory system (100) including a non-volatile flash memory, and also including code devices (716) stored in a memory area (128) of the system. (See Page 8, line 19-Page 13, line 26; Page 18, lines 9-19; and Page 20, lines 1-6). These code devices (716) include code devices that divide a page of the flash memory into at least two segments (See Figs 4a-4c and Page 13, line 27-Page 16, line 18), and code devices that encode a first one of the segments according to a first ECC algorithm, and that encode a second segment according to a second ECC algorithm. (See Page 20, line 29-Page 21, line 3). Code devices (720) for programming the page of the flash memory, the page being the smallest unit of programming, with the encoded data for the first and second segments are also provided in the system.

Independent claim 23 is also directed to a memory system (100) including a non-volatile memory (124). (See Page 8, line 19-Page 13, line 26). The memory system of claim 23 includes means (128; 716) that divide at least part of a page of the non-volatile memory into two or more segments, and means that perform error correction code calculations on a first segment according to a first ECC algorithm,

and separately upon a second segment according to a second ECC algorithm. (See Page 8, line 19-Page 13, line 26; Page 18, lines 9-19; Page 20, lines 1-6; and Page 20, line 29-Page 21, line 3). Means (19; 720) for programming the page with the encoded data for the first and second segments are also provided in the system. (See Page 11, line 22–Page 12, line 16).

The claimed invention, in both its method and system form, provides important advantages over conventional flash memory systems. As known in the art, error correction coding impacts the data storage capacity, because such coding requires some number of bits to store redundant information used to detect and correct errors in the payload data. Higher capability error correction codes (*i.e.*, codes that correct a higher number of errors for a given data block size) require more computational overhead and also more memory bits to store the redundant data, as compared with lower capability codes. (See Page 3, lines 1-8 and Page 7, line 4-13). The claimed method and systems, and their ability to use different ECC codes for different portions of the same page, provide great flexibility in the optimizing of error correction performance, for example in the storage of information of differing sensitivity to error, and improved efficiency in using more complex ECC operations only to the extent necessary for the desired error correction capability.

Claims Appendix

1. A method for storing data associated with a page within a non-volatile flash memory of a memory system, the page being the smallest unit of programming in the non-volatile flash memory, and having a data area and an overhead area, the method comprising:

dividing at least a part of the page into at least a first segment and a second segment;

encoding data associated with the first segment according to a first error correction code (ECC) algorithm;

encoding data associated with the second segment according to a second ECC algorithm, wherein the data associated with the second segment is encoded substantially separately from the data associated with the first segment; and

programming the page with the encoded data associated with the first and second
segments.

2. The method of claim 1 wherein the first segment includes the data area and the second segment includes the overhead area.

3. The method of claim 1 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

4. The method of claim 1 wherein the first ECC algorithm is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.

5. The method of claim 4 wherein the first ECC algorithm is a Hamming Code ECC algorithm.

6. The method of claim 1 wherein dividing the at least part of the page into the at

least two segments of the data includes:

dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.

7. The method of claim 6 further including:

performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment and the second segment.

8. The method of claim 6 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.

9. The method of claim 6 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

10. The method of claim 1 wherein the non-volatile flash memory is one of a NAND flash memory and an MLC NAND flash memory.

11. A memory system comprising:

a non-volatile flash memory, the non-volatile flash memory including a page, the page being the smallest unit of programming in the non-volatile flash memory, and having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data;

code devices for dividing at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment;

code devices for encoding data associated with the first segment according to a first error correction code (ECC) algorithm and for encoding data associated with the second segment according to a second ECC algorithm, wherein the data associated with the

second segment is encoded substantially separately from the data associated with the first segment;

code devices for programming the page with the encoded data associated with the first and second segments; and

a memory area for storing the code devices.

12. The memory system of claim 11 further including: a controller, the controller being arranged to process the code devices.

13. The memory system of claim 11 wherein the first segment includes the data area and the second segment includes the overhead area.

14. The memory system of claim 11 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

15. The memory system of claim 11 wherein the first ECC algorithm is arranged to detect up to two incorrect bits and to correct up to one of the incorrect bits in each of the first segment and the second segment.

16. The memory system of claim 15 wherein the first ECC algorithm is a Hamming Code ECC algorithm.

17. The memory system of claim 11 wherein the code devices for dividing the at least part of the page into the at least two segments include:

code devices for dividing the page into three segments, the three segments including the first segment, the second segment, and a third segment.

18. The memory system of claim 17 further including:

code devices for performing the ECC calculations on the third segment according to one of the first and second ECC algorithms to encode the third segment, wherein the third segment is encoded substantially separately from the first segment

and the second segment.

19. The memory system of claim 17 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.

20. The memory system of claim 17 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

21. The memory system of claim 11 wherein the non-volatile flash memory is one of a NAND flash memory and an MLC NAND flash memory.

22. The memory system of claim **11** wherein the code devices are one of software code devices and firmware code devices.

23. A memory system comprising:

a non-volatile flash memory, the non-volatile flash memory including a page, the page being the smallest unit of programming in the non-volatile flash memory, and having a data area and an overhead area, the data area and the overhead area being arranged to contain bits of data;

means that divide at least a part of the page into at least two segments, the at least two segments including a first segment and a second segment;

means that encode data associated with the first segment according to a first error correction code (ECC) algorithm and that encode data associated with the second segment according to a second ECC algorithm,

means for programming the page with the encoded data associated with the first and second segments; and

wherein the second segment is encoded substantially separately from the first segment.

24. The memory system of claim 23 wherein the first segment includes the data area and the second segment includes the overhead area.

25. The memory system of claim 23 wherein the first segment includes a first section of the data area and the second segment includes a second section of the data area.

27. The memory system of claim 23 wherein the means that divide the at least part of the page into the at least two segments include:

means that divide the page into three segments, the three segments including the first segment, the second segment, and a third segment.

28. The memory system of claim 27 further including:

means that perform the ECC calculations according to one of the first and second ECC algorithms on the third segment to encode the third segment,

wherein the third segment is encoded substantially separately from the first segment and the second segment.

29. The memory system of claim 27 wherein the first segment includes a first section of the data area, the third segment includes a second section of the data area, and the second segment includes the overhead area.

30. The memory system of claim 27 wherein the first segment includes a first section of the data area, the second segment includes a second section of the data area, and the third segment includes a third section of the data area.

31. The memory system of claim 23 wherein the non-volatile flash memory is one of a NAND flash memory and an MLC NAND flash memory.

REMARKS

If there are any questions regarding the substitute Summary of the Claims Subject Matter and Claims Appendix sections, the Examiner is asked to phone the undersigned attorney at (312) 321-4200.

Respectfully submitted,

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